REMARKS

Reconsideration of this application is respectfully requested in view of the following remarks. Claims 1-10 are currently pending in the application and subject to examination.

Claims 1-10 Recite Patentable Subject Matter

In the Office Action mailed December 13, 2005, claims 1-10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,858,190 to Yamaguchi et al. (hereinafter, "Yamaguchi") in view of U.S. Patent No. 5,282,164 to Kawana (hereinafter, "Kawana"). The Applicant traverses the rejection, as follows.

In the present invention as claimed, a data shifting unit holds and shifts data, and an address signal specifies which column of the shifting unit functions as an input column.

In Yamaguchi, however, as shown in Fig. 2, the shift register USR does not hold and shift data, but holds and shifts an address signal decoded by the column decoder C-DCR.

Specifically, in Yamaguchi, one of signals Y0, Y1, ...Yn is selected and set in the column decoder C-DCR. Here, assuming that a signal Ym is selected and set in the column decoder C-DCR, when a clock Φ is input once, a switch associated with signal Ym turns on, and then data is sent to the corresponding latch UDFF via data bus SIO. Then, when another clock Φ is input, the shift register USR conducts the shifting action to be set to the signal Ym+1, a switch associated with signal Ym+1 turns on, and then data is sent to the corresponding latch UDFF (m+1) via data bus SIO. In this way, the address signal held in the shift register USR shifts in accordance with the clock Φ, and

thus the corresponding column is selected in succession. Therefore, the configuration of the shift register of Yamaguchi is similar to the configuration of an address counter 150 shown in Fig. 3 of the present application, which illustrates a prior art configuration, in the specification as filed.

Kawana merely discloses a serial-to-parallel converter similar to the shift register 120 shown in Fig. 1 of the present application, which illustrates a prior art configuration, in the specification as filed.

Thus, the configuration of Yamaguchi substantially corresponds to the prior art configuration of Fig. 3 of the present application, and the configuration of Kawana substantially corresponds to the prior art configuration of Fig. 1 of the present application. The disadvantages of the prior art configurations shown in Figs. 1 and 3 of the subject application are described in the "Description of the Related Art" section of the application. The claimed invention, in which a data shifting unit holds and shifts data, and an address signal specifies which column of the shifting unit functions as an input column, overcomes such disadvantages of the prior art.

As the combination of the prior art shown in Figs. 1 and 3 of the specification does not yield the claimed invention, or provide the benefits thereof, neither does the combination of Yamaguchi and Kawana.

For at least these reasons, the Applicant submits that the cited combination of references neither discloses nor suggests at least the combination of a data shifting unit including a plurality of columns, and sequentially shifting the input serial data through the plurality of columns; and a selection unit selecting a column among the plurality of columns as an input column by following the address signal, wherein the input serial

data is inputted to said data shifting unit through the input column, as recited in claims 1 and 8. Thus, the Applicant submits that independent claims 1 and 8 are allowable over the combination of Yamaguchi and Kawana. As claims 1 and 8 are allowable, the Applicant submits that claims 2-7 and 9, which depend from allowable claims 1 and 8, respectively, are likewise allowable.

Similarly, the Applicant submits that the cited combination of references neither discloses nor suggests at least the combination of selecting a column among a plurality of columns of a data shifting unit as an input column by following the address signal; inputting the input serial data to said data shifting unit through the input column; and shifting the input serial data sequentially through the plurality of columns, as recited in claim 10. For at least this reason, the Applicant submits that claim 10 is allowable.

Conclusion

For all of the above reasons, it is respectfully submitted that claims 1-10 are in condition for allowance and a Notice of Allowability is earnestly solicited.

Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is invited to contact the undersigned representative at the telephone number listed below.

In the event this paper is not considered to be timely filed, the Applicant hereby petitions for an appropriate extension of time. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300 referencing client matter number 100353-00040.

Respectfully submitted,

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Enclosure: Petition for Extension of Time